# Hi-Flex AMIBIOS

# for the

# SIS EISA 80486

# Chipset

## User's Guide

Based on the 06/06/92 core AMIBIOS.
Use with AMIBCP Version 2.1.

MAN486DXSISEISA
1/9/93

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## Revision History

| | |
|---|---|
| 8/6/92 | Initial release. |
| 11/23/92 | Updated for 06/06/92 core AMIBIOS. |
| 1/9/93 | Updated for minor AMIBIOS modifications. |

# Table of Contents

# Preface

## To the OEM Reader

The Hi-Flex AMIBIOS is a state of the art product which includes major engineering innovations. The Hi-Flex AMIBIOS can be easily configured by the OEM, system integrator, or VAR building systems that include the AMIBIOS through the AMIBIOS Configuration Program (AMIBCP). See the *AMIBCP User's Guide* for detailed information.

This manual was written for the OEM to assist in the proper use of the AMIBIOS Setup utility. This manual is not meant to be read by the computer owner who purchases a computer with the AMIBIOS. It is assumed that the computer manufacturer will use this manual as a sourcebook of information, and that parts of this manual will be included in the computer owner's manual. It is also assumed that the OEM, VAR, or system integrator that is reading this manual has also licensed the right to use the AMIBIOS technical documentation.

### Technical Support

If an AMIBIOS fails to operate as described or you need more information, call technical support at 404-246-8600. Make sure you have the following information before calling technical support:

- Serial number and revision number of the BIOS
- System BIOS reference number
- A clear description of the problem.

### Acknowledgments

This manual was written and edited by Paul Narushoff and Robert Cheng. The writers gratefully acknowledge the assistance of the BIOS engineers.

### BIOS File

This manual documents AMIBIOS file SISEISAP.ROM.

# Chapter 1

# Introduction

This manual documents the AMIBIOS for the SIS (Silicon Integrated Systems) EISA Chipset. Please see the SIS technical documentation for additional information.

### New AMIBIOS Features

The following features have been added to the AMIBIOS for the SIS EISA chipset:

- added support for 1 MB of cache mempry, as well as 64 KB, 128 KB, 256 KB, and 512 KB of cache.
- now supports 16 MB x 9 SIMMs at all frequencies of operation.

### System BIOS

The BIOS is the basic input output system used in all IBM® PC-, XT™-, AT®-, and PS/2®- compatible computers. The Hi-Flex AMIBIOS is a high-quality example of a system BIOS.

### Configuration Data

AT-Compatible systems, also called ISA (Industry Standard Architecture) systems, and EISA (Extended Industry Standard Architecture) systems must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-Compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

EISA systems have at least 4 KB of additional CMOS RAM to store EISA configuration information.

### How Data Is Configured

The AMIBIOS provides a BIOS Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup is used to set configuration data in CMOS RAM.

### Types of AMIBIOS Setup

There are five types of Setup in the AMIBIOS:

| Types of Setup | Description |
|---|---|
| STANDARD CMOS SETUP | Sets time, date, hard disk type, types of floppy drives, monitor type, and if keyboard is installed. These options are documented in the *Hi-Flex AMIBIOS User's Guide*. |
| ADVANCED CMOS SETUP | Sets Typematic Rate and Delay, Above 1 MB Memory Test, Memory Test Tick Sound, Hit <Del> Message Display, System Boot Up Sequence, and many others. These options are documented in the *Hi-Flex AMIBIOS User's Guide*. |
| ADVANCED CHIPSET SETUP | Sets chipset-specific options and features. The ADVANCED CHIPSET SETUP options for the AMIBIOS for the SIS EISA Chipset are documented on pages through . |
| Power Management Setup | Sets power conversion features for laptop computers. It is not available in the AMIBIOS for the SIS EISA Chipset. |
| Peripheral Setup | Sets features related to Integrated Peripheral Controllers. It is not in the AMIBIOS for the SIS EISA Chipset. |

### Reference

STANDARD CMOS SETUP and the common ADVANCED CMOS SETUP options are described in the *Hi-Flex AMIBIOS User's Guide*. ADVANCED CHIPSET SETUP is described in this manual.

### Advanced BIOS Features

The ROM file for the AMIBIOS for the SIS EISA chipset enable Clock Switching and Cache Control through chipset registers in AMIBCP. It does not use the Turbo Switch Input Pin or Reset Memory Controller AMIBCP options.

# EISA Characteristics

The Extended Industry Standard Architecture (EISA) is a 32-bit extension to the Industry Standard Architecture (ISA) that supports current and future high performance application environments.

EISA is fully compatible with ISA (sometimes called AT-compatible) and delivers 32-bit I/O capabilities for high performance data transfer. EISA is a superset of the industry standard 8/16-bit ISA I/O bus.

EISA builds on the existing standard. In addition to standard ISA signals, EISA slots have signals that support 32-bit EISA adapter cards.
The 32-bit EISA expansion slots are fully compatible with 8-bit and 16-bit PC/XT/AT adapter cards.

**EISA Slots**

EISA slots have 188 pins. The top 98 pins are exactly the same as the standard AT pinouts. The bottom 90 pins are used for the EISA signal.

**EISA Bus is much faster than ISA Bus**

Not only does EISA provide a wider 32-bit bus, it also provides a maximum 33 MB/sec bus transfer rate. The ISA bus transfers data at only 8 MB/sec.

# EISA Characteristics, Continued

## EISA and ISA Bus Rates

| Attribute | EISA Bus | ISA Bus |
|---|---|---|
| Burst Transfer Rate | 33 MB/second. | 8 MB/second at 0 wait states. |
| DMA characteristics | Supports 8-, 16-, and 32-bit DMA. | Supports 8- and 16-bit DMA. |
| DMA Transfer Rate | Up to 33 MB/second. | 1 to 4 MB/seconds. |
| Expansion Card Pin Count | 188 pins. | 98 pins. |
| Bus Master | Multiple bus master. | No bus mastering. |
| Configuring Expansion Cards | Autoconfiguration through ECU. DIP switch and Jumper setting still available. | Only DIP Switch and jumper setting available. |

# Features

## BIOS Information

The following graphic shows the AMIBCP BIOS Information.

### BIOS Options

The following graphic illustrates the AMIBCP BIOS Options for this AMIBIOS file.

### Miscellaneous BIOS Features

The following screen shows the AMIBCP Miscellaneous options for this BIOS file.

# Chapter 2

# ADVANCED CMOS SETUP

## Default Settings

Every option in AMIBIOS Setup contains two default values: a power-on default and the BIOS Setup default value.

### The Power-on Defaults

The power-on default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

### Setup Defaults

The BIOS Setup default values provide optimum performance settings for all devices and system features.

## ADVANCED CMOS SETUP Options

The ADVANCED CMOS SETUP options for the AMIBIOS for the SIS EISA Chipset Support are the same as the standard AMIBIOS ADVANCED CMOS SETUP options, documented in the *Hi-Flex AMIBIOS User's Guide*.

# Chapter 3

# ADVANCED CHIPSET SETUP

This chapter describes the ADVANCED CHIPSET SETUP options for the AMIBIOS for the SIS EISA Chipset. Refer to the documentation provided by SIS for additional assistance in understanding specific chipset options.

**ADVANCED CHIPSET SETUP Screen**

## Default Settings

Every option in AMIBIOS Setup contains two default values: a power-on default and the BIOS Setup default value.

## Default Settings, Continued

### The Power-on Defaults

The power-on default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

### Setup Defaults

The BIOS Setup default values provide optimum performance settings for all devices and system features.

### Configuring Advanced Chipset Options

The OEM can choose the options that are included in the ADVANCED CHIPSET SETUP part of the AMIBIOS Setup utility through AMIBCP. The OEM can also add additional options. See the *AMIBCP User's Guide* for additional information.

## ADVANCED CHIPSET SETUP Options

### DRAM Speed

The settings are listed in the table below. The BIOS and Power-on defaults are *Slowest.*

| **Setting** | **CPU Speed** |
|---|---|
| *Slowest* | 25 MHz |
| *Slower* | 33 MHz |
| *Faster* | 40 MHz |
| *Fastest* | 50 MHz |

**DRAM Write CAS Pulse Width**

The settings are *2T* or *1T.* The BIOS and Power-on defaults are *2T.*

**DRAM Interleave**

If enabled, DRAM is interleaved. This option is valid only if there are two or four DRAM banks. The settings are *Enabled* or *Disabled.* The BIOS default is *Enabled.* The Power-on default is *Disabled.*

**Cache Write Back**

The settings are *Enabled* (Write-Back) or *Disabled* (Write-Through). The BIOS and Power-on defaults are *Disabled.*

**Cache Write Cycle**

The settings are *3T* or *2T.* The BIOS and Power-on defaults are *3T.*

**Cache Burst Read Cycle**

The settings are *1T* or *2T.* The BIOS and Power-on defaults are *1T.*

**KBCLK Selection**

This option sets the source for the keyboard clock. The settings are *BUSCLK* or *Faster.* The BIOS and Power-on defaults are *BUSCLK.*

**BUSCLK Selection**

The settings are listed in the following table. The BIOS and Power-on defaults are *7.159 MHz.*

| **Setting** | **CPU Speed** |
|---|---|
| *7.159 MHz* | 7.159 MHz |
| *CPUCLK/8* | 66 MHz |
| *CPUCLK/6* | 50 MHz |
| *CPUCLK/5* | 40 MHz |
| *CPUCLK/4* | 33 MHz |
| *CPUCLK/3* | 25 MHz |
| *CPUCLK/2.5* | 20 MHz |
| *CPUCLK/2* | 16 MHz |

**Non-Cacheable Area 1**
**Non-Cacheable Area 2**

The settings are *DRAM* or *ATBUS.* The BIOS and Power-on defaults are *DRAM.*

**Non-Cacheable Area 1 Size**
**Non-Cacheable Area 2 Size**

These options define the size of two areas of memory (Area 1 and Area 2) that cannot be cached. The settings are *0 KB, 64 KB, 128 KB, 256 KB, 512 KB, 1 MB, 2 MB,* or *4 MB.* The BIOS and Power-on defaults are *0 KB.*

**Non-Cacheable Area 1 Start**
**Non-Cacheable Area 2 Start**

These options define the beginning of the two areas of memory whose contents cannot be cached. The BIOS and Power-on defaults are *Disabled.*

**C000 Shadow RAM Cacheable**

This option, when enabled, permits the contents of the C0000h-C7FFFh memory area to be cached. You must make sure that no program the system will be running will write to this area before you enable caching in this area. The settings are *Enabled* or *Disabled.* The BIOS and Power-on defaults are *Disabled.*

**F000 Shadow RAM Cacheable**

This option, when enabled, permits the contents of the F0000h-FFFFFh memory area (the system BIOS) to be cached. You must make sure that no program the system will be running will write to this area before you enable caching in this area. The settings are *Enabled* or *Disabled.* The BIOS and Power-on defaults are *Disabled.*

**I/O Recovery Select**

The settings are *3 BCLKs, 4 BCLKs, 5 BCLKs,* or *11 BCLKs.* The BIOS and Power-on defaults are *11 BCLKs.*

**Fast Reset Emulation Select**

The settings are *Enabled* or *Disabled.* The BIOS and Power-on defaults are *Enabled.*

**Fast Reset Emulation Mode**

This option sets the delay before a RESET is sent. The settings are *6 µS* or *2 µS.* The BIOS and Power-on defaults are *6 µS.*

# Chapter 4

# CMOS Map

A map of CMOS RAM as configured by the AMIBIOS for the SIS EISA Chipset is shown in the following table.

| CMOS Location | Description |
|---|---|
| 00h - 0Fh | Standard IBM AT compatible RTC and Status Register data definitions. |
| 10h | Floppy Drive Type<br>Bits 7-4 Drive A: Type<br>0 No Drive<br>1 360 KB Drive<br>2 1.2 MB Drive<br>3 720 KB Drive<br>4 1.44 MB Drive<br>Bits 3-0 Drive B: Type (bit settings same as A) |
| 11h | Bit 7 Mouse Support Option<br>Bit 6 Above 1 MB Memory Test<br>Bit 5 Memory Test Tick Sound<br>Bit 4 Memory Parity Error Check<br>Bit 3 Hit <DEL> Message Display<br>Bit 2 Hard Disk Type 47 RAM Area<br>Bit 1 Wait for <F1> If Any Error<br>Bit 0 System Boot Up Num Lock |
| 12h | Hard Disk Data<br>Bits 7-4 Hard Disk Drive C: Type<br>0 No drive<br>1-14 Hard drive Type 1-14<br>16 Hard Disk Type 16-255 (actual Hard Drive Type is in CMOS RAM 1Ah)<br>Bits 3-0 Hard Disk Drive D: Type (Same as C:) |
| 13h | Keyboard Typematic Data<br>Bit 7 Enable Typematic (1 = On)<br>Bits 6-5 Typematic Delay<br>00b 250 ms<br>01b 500 ms<br>10b 750 ms<br>11b 100 ms<br>Bits 4-0 Typematic Rate<br>0 - 300 8 - 159 16 - 75 24 - 37<br>1 - 267 9 - 133 17 - 67 25 - 33<br>2 - 240 10 - 120 18 - 60 26 - 30<br>3 - 218 11 - 109 19 - 55 27 - 27 |

| | |
|---|---|
| | 4 - 200 12 - 100 20 - 50 28 - 25<br>5 - 185 13 - 92 21 - 46 29 - 23<br>6 - 171 14 - 86 22 - 43 30 - 21<br>7 - 160 15 - 80 23 - 40 31 - 20 |
| 13h | Advanced Setup Options<br>Bit 7 Mouse Enabled (1 = On)<br>Bit 6 Test Memory above 1 MB (1 = On)<br>Bit 5 Memory Test Tick Sound (1 = On)<br>Bit 4 Memory Parity Error Check (1 = On)<br>Bit 3 Press <Esc> to Disable Memory Test (1 = On)<br>Bit 2 User-Defined Hard Disk (1 = On)<br>Bit 1 Wait for <F1> Message if Error (1 = On)<br>Bit 0 Turn Num Lock Off at boot (1 = On) |
| 14h | Equipment Byte<br>Bits 7-6 Number of Floppy Drives<br>00b 1 Drive<br>01b 2 Drives<br>Bits 5-4 Monitor Type<br>00b Not CGA or MDA<br>01b 40x25 CGA<br>10b 80x25 CGA<br>11b MDA (Monochrome)<br>Bit 3 Display Enabled (1 = On)<br>Bit 2 Keyboard Enabled (1 = On)<br>Bit 1 Math coprocessor Installed (1 = On)<br>Bit 0 Floppy Drive Installed (0 = On) |
| 15h | Base Memory (in 1K increments), Low Byte |
| 16h | Base Memory (in 1K increments), High Byte |
| 17h | Extended Memory (in 1K increments), Low Byte |
| 18h | Extended Memory (in 1K increments), High Byte (Max 15 MB) |
| 19h | Hard Disk C: Drive Type<br>16-255 Hard Drive Type 16-255 |
| 1Ah | Hard Disk D: Drive Type (Same as Drive C: above) |
| 1Bh | User-Defined Drive C: - # of Cylinders, Low Byte |
| 1Ch | User-Defined Drive C: - # of Cylinders, High Byte |
| 1Dh | User-Defined Drive C: - Number of Heads |
| 1Eh | User-Defined Drive C: - Write Precompensation Cylinder, Low Byte |
| 1Fh | User-Defined Drive C: - Write Precompensation Cylinder, High Byte |
| 20h | User-Defined Drive C: - Control Byte (80h if # of heads is equal or greater than 8) |
| 21h | User-Defined Drive C: - Landing Zone, Low Byte |
| 22h | User-Defined Drive C: - Landing Zone, High Byte |
| 23h | User-Defined Drive C: - # of Sectors |
| 24h | User-Defined Drive D: - # of Cylinders, Low Byte |

| | |
|---|---|
| 25h | User-Defined Drive D: - # of Cylinders, High Byte |
| 26h | User-Defined Drive D: - Number of Heads |
| 27h | User-Defined Drive D: - Write Precompensation Cylinder, Low Byte |
| 28h | User-Defined Drive D: - Write Precompensation Cylinder, High Byte |
| 29h | User-Defined Drive D: - Control Byte (80h if # of heads is equal or greater than 8) |
| 2Ah | User-Defined Drive D: - Landing Zone, Low Byte |
| 2Bh | User-Defined Drive D: - Landing Zone, High Byte |
| 2Ch | User-Defined Drive D: - # of Sectors |
| 2Dh | Configuration Options<br>Bit 7 Slow DRAM Mode (1 = On)<br>Bit 6 Floppy Drive Seek - turn off for fast boot<br>Bit 5 Boot Order 0 - Drive C:, then A:<br>1 - Drive A:, then C:<br>Bit 4 Boot Speed (0 - Low; 1 - High)<br>Bit 3 External Cache Enable (1 = On)<br>Bit 2 Internal Cache Memory (1 = On)<br>Bit 1 Use Fast Gate A20 after boot (1 = On)<br>Bit 0 Turbo Switch (1 = On) |
| 2Eh | Standard CMOS Checksum, High Byte |
| 2Fh | Standard CMOS Checksum, Low Byte |
| 30h | Extended Memory, Low Byte |
| 31h | Extended Memory, High Byte (Maximum 15 MB) |
| 32h | Century Byte (BCD value for the century) |
| 33h | Information Flag |
| 34h | Shadowing<br>Bit 6 Password Checking Option<br>Bit 5 C8000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 4 CC000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 3 D0000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 2 D4000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 1 D8000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 0 DC000h Shadow Adaptor ROM (Bit 1 = On) |
| 35h | Shadowing<br>Bit 7 E0000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 6 E4000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 5 E8000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 4 EC000h Shadow Adaptor ROM (Bit 1 = On)<br>Bit 3 F0000h Shadow System ROM (Bit 1 = On)<br>Bit 2 C0000h Shadow Video ROM (Bit 1 = On)<br>Bit 1 C4000h Shadow Video ROM (Bit 1 = On) |
| 36h | Bit 1 Auto Configuration<br>Bit 0 DRAM Interleave |
| 38h - 3Dh | Encrypted Password |

| | |
|---|---|
| 3Eh | Extended CMOS Checksum, High Byte (includes 34h - 3Dh) |
| 3Fh | Extended CMOS Checksum, Low Byte (includes 34h - 3Dh) |

# Extended CMOS RAM

| CMOS Location | Description | |
|---|---|---|
| 40h-48h | Reserved | |
| 49h | Bits 1-0 | I/O Recovery Select |
| 4Ah-4Ch | Reserved | |
| 4Dh | Bit 2<br>Bit 1 | Fast Reset Emulation Mode<br>Fast Reset Emulation Select |
| 4Eh-5Fh | Reserved | |
| 60h | Bits 7-6<br>Bit 5 | DRAM Speed<br>DRAM Write CAS Pulse Width |
| 61h | Bit 6<br>Bit 1<br>Bit 0 | Cache Write Back<br>Cache Write Cycle<br>Cache Burst Read Cycle |
| 62h | Reserved | |
| 63h | Bit 3<br>Bits 2-0 | KBCLK Selection<br>BUSCLK Selection |
| 64h | Bit 7<br>Bits 6-4 | Non-Cacheable Area 1<br>Non-Cacheable Area 1 Size |
| 65h | Bits 7-0 | Non-Cacheable Area 1 Start |
| 66h | Bit 7<br>Bits 6-4 | Non-Cacheable Area 2<br>Non-Cacheable Area 2 Size |
| 67h | Bits 7-0 | Non-Cacheable Area 2 Start |
| 68h | Bit 2<br>Bit 1 | F000 Shadow RAM Cacheable<br>C000 Shadow RAM Cacheable |
| 69h-7Fh | Reserved | |

# Chapter 5

## Chipset Registers

The AMIBIOS for the SIS EISA chipset sets the following bits in the following chipset registers.

| Register | Description |
|---|---|
| 00h-08h | Reserved |
| 09h | Bits 1-0 I/O Recovery Select<br>00 3 BCLKs 01 4 BCLKs<br>10 5 BCLKs 11 11 BCLKs |
| 0Ah-0Ch | Reserved |
| 0Dh | Bit 2 Fast Reset Emulation Mode<br>0 6 us<br>1 2 us<br>Bit 1 Fast Reset Emulation Select<br>0 Disabled<br>1 Enabled |
| 60h | 7-6 DRAM Speed<br>00 Slowest 01 Slower<br>10 Faster 11 Fastest<br>5 DRAM Write CAS Pulse Width<br>0 2T<br>1 1T |
| 61h | 6 Cache Write Burst<br>0 Disabled<br>1 Enabled<br>1 Cache Write Cycle<br>0 3T<br>1 2T<br>0 Cache Burst Read Cycle<br>0 1T<br>1 2T |
| 62h | Reserved |
| 63h | 3 KBCLK Selection<br>0 BUSCLK<br>1 Faster<br>2-0 BUSCLK Selection<br>000 7.159MHz 001 CPUCLK/8<br>010 CPUCLK/8 011 CPUCLK/5<br>100 CPUCLK/4 101 CPUCLK/3<br>110 CPUCLK/2.5 111 CPUCLK/2 |
| 64h | 7 Non-Cacheable Area 1<br>0 DRAM |

| | |
|---|---|
| | 1 ATBUS<br>6-4 Non-Cacheable Area 1 Size<br>000 0 KB 001 64 KB<br>010 128 KB 011 256 KB<br>100 512 KB 101 1 MB<br>110 2 MB 111 4 MB |
| 65h | Non-Cacheable Area 1 Start |
| 66h | 7 Non-Cacheable Area 2<br>0 DRAM<br>1 ATBUS<br>6-4 Non-Cacheable Area 2 Size<br>000 0 KB 001 64 KB<br>010 128 KB 011 256 KB<br>100 512 KB 101 1 MB<br>110 2 MB 111 4 MB |
| 67h | Non-Cacheable Area 2 Start |
| 68h | 2 F000 Shadow RAM Cacheable<br>0 Disabled<br>1 Enabled<br>1 C000 Shadow RAM Cacheable<br>0 Disabled<br>1 Enabled |

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